

**Abstract of the Disclosure**

A highly integrated semiconductor device operates at a high speed due to low resistance at the gate electrode and minimal parasitic capacitance between the gate electrode and substrate. A gate pattern is formed on a substrate, and an insulating layer is formed over the substrate including over the gate pattern. The thickness of the insulating layer is reduced until the upper surface thereof beneath the level of the upper surface of the gate electrode. A conductive layer is then formed on the substrate, and is anisotropically etched to thereby form wings constituting a first spacer on upper sidewalls of the gate pattern. Then, the insulating layer is etched to leave a portion thereof beneath the wings. This remaining portion of the insulating layer constitutes a capacitance preventative layer that serves as a measure against the subsequent forming of a parasitic capacitor when source/drain electrodes are formed by implanting ions into the substrate and heat-treating the same.